instruction set

Mnemonic *Description*

Memory reference instruction

	LD	Load register
	ST	Store register
	AD	Addition
	SU	Subtract
	AN	Logical and
	OR	Logical or
	XR	Exclusive or
	IM	Increment memory
	C2	Two's complement
*	ML	Multiple load
*	MS	Multiple store
	ABI	Absolute conditional branch
	CFI	Call function
	C1	One's complement
	CW	Compare word
*	CC	Compare character
	LC	Load character
	SC	Store character
	RF	Relative Forward conditional branch
	RB	Relative Backward conditional branch
**	MU	Multiply
**	DV	Divide
**	DA	Double Add
**	DS	Double Subtract

Register to register instructions

	LDR	Load register/register
	STR	Store register/register
	ADR	Addition register/register
	SUR	Subtract register/register
	ANR	AND register/register
	TM	Test Mask
	TNM	Test Not Mask
	ORR	OR register/register
	XRR	XOR register/register
	IMR	Increment memory/register
	C2R	Two's complement register
*	MLR	Multiple load/register
*	MSR	Multiple Store/register
	ABR	Absolute conditional branch/register
	CFR	Call Function/register
	C1R	One's complement register
	CWR	Compare word register/register
*	CCR	Compare character/Register
	LCR	Load character/Register
	SCR	Store character/Register
	RTN	Return
	ECR	Exchange character register/register
**	MUR	Multiply
**	DVR	Divide
**	DAR	Double Add
**	DSR	Double subtract

Constant instructions

	LDK	Load constant
	ADK	Add constant
	SUK	Subtract constant
	ANK	Logical and with constant
	ORK	Logical or with constant
	XRK	Exclusive or with constant
*	MLK	Multiple load constant
	AB	Absolute conditional branch
	CF	Call function
	CWK	Compare word with constant
*	CCK	Compare character
	LCK	Load character
**	MUK	Multiply with constant
**	DVK	Divide with constant
**	DAK	Double add with constant
**	DSK	Double subtract with constant

Shift instructions

°*	SLA	Shift left arithmetic
°*	SRA	Shift right arithmetic
°*	SLL	Shift left logical
*	SRL	Shift right logical
*	SLC	Shift left circular
°*	SRC	Shift right circular
*	SLN	Shift left normalize
*	SRN	Shift right normalize
*	DLA	Double length left arithmetic shift
*	DRA	Double length right arithmetic shift
*	DLL	Double length left logical shift
*	DRL	Double length right logical shift
*	DLC	Double length left circular shift
*	DRC	Double length right circular shift
*	DLN	Double length left and normalize
*	DRN	Double length right and normalize

I/O Instructions

	CIO	Control I/O
	INR	Input to register
	SST	Send status
	OTR	Output from register
	TST	Test status
**	WMP	Write Mask Protection
1	WM2	Write mask 2
	RIL	Read Interrupt Line
	WIM	Write Interrupt Mask

Miscellaneous instructions

	ENB	Enable interrupt
	HLT	Halt
	RIT	Reset internal interrupts
	INH	Inhibit interrupt
	LKM	Link to monitor
*	SMD	Set mode

* P855 and P860 - standard
** P855 and P860 - option
° These instructions are available with the P850 but will only shift one position.
1 This is for use with P860 machines with greater than 16k memory.

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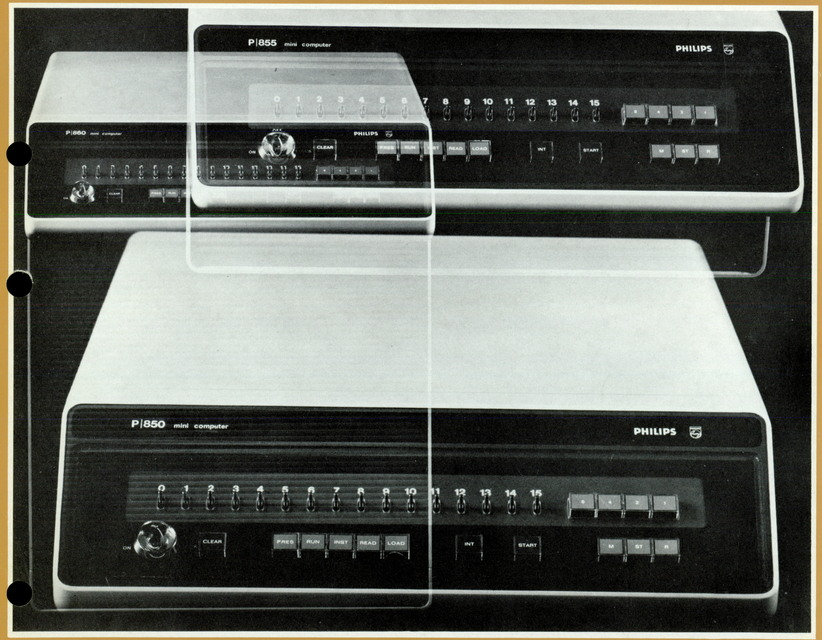
PHILIPS

software P850/P855/P860



PHILIPS data systems

The new Philips family of mini computers has impressive specifications and looks extremely attractive. However, there is one aspect of any computer system that is of the utmost importance in deciding whether it will do what you want it to. That is software.

The only limitation in compatibility between machines in the Philips family is memory size. The minimum memory size is indicated in the title of the package. In software as well as in hardware, Philips is among the leaders in the mini computer business.

system monitors

1k Executive System
This is a highly modular package that furnishes a number of program development and run-time facilities. It can contain a bootstrap loader for loading programs in absolute object code format; a program loader; utility routines for a binary or hexadecimal core dump; I/O routines for reading or writing in binary or ASCII; interrupt handling routines; and arithmetic routines which simulate optional hardware instructions for multiply, divide, double add and double subtract.

4k Basic Monitor
Single task supervisor with I/O handling and a subset of the system macro calls available on the larger real-time monitor. Usable at program generation time as well as at run time. It includes a scheduled label facility for intertask synchronization.

8k Real-time Monitor
This is a multitask system that utilizes 48 hardware interrupt levels and 16 software priority levels. The system handles all I/O requests and interrupts. Facilities are available via operator command or system macro calls. They include the ability to connect programs to software levels and timers, allowing mutitasking and program activation under control of a timer. I/O handling is done by the monitor, a wide variety of functions being available. A background area can be defined to utilize spare CPU time when no foreground task is active. The memory protection feature can be utilized for a very high degree of program security. Fast fixed head disc can be used to store disc resident programs.

8k Disc Operating System
This keyboard oriented operating system allows program generation and testing. The required disc holds, in addition to user files, all the system software components including Text Editor, Assemblers and compiler Linkage Editors and Debug Program.

programming languages

Stand-alone Assembler
This is one of the smallest assemblers in the world. It functions in only 2k of store but it accepts the full instruction set of the P850 and needs only one pass. Input is in restricted assembler source language; output is in absolute or relocatable object code.
Acceptable directives are: – IDENT, EQU, RES, AORG, RORG, END and DATA.
There is an optional listing suppression and normal 'Halt on error'.

4k Stand-alone Assembler
This is a one pass assembler that outputs absolute or relocatable object code.
Facilities are as follows; external references allowed; non-permanent update; non-fatal error recovery procedure; optional inclusion of symbol table in generated code; double buffered I/Os for configurations greater than 4k.
Acceptable directives are ENTRY, EXTeRNal and COMmoN for linkage control, plus IDENTification, EQUivalence, REServe, (N)LIST, assign Absolute ORiGin, assign Relocatable ORiGin, Symbol TABle, END and DATA.

8k Macro Assembler
This is an extended version that provides macro and conditional assembly features. The additional assembly directives are FORM, XFORM, GENerate, EJECT page, IF False, IF True and XIF (finish conditional assembly).

4k FORTRAN Compiler
Although this compiler will function efficiently in only 4k of store, it is still an advance on basic USASI FORTRAN. It is a one pass compiler that generates code for interpretation at run time. This is done for economy of store space at run time. A comprehensive subroutine library is available.

8k FORTRAN Compiler
This accepts full USASI FORTRAN IV and can generate (optionally) interpretive object code for economical store use, or directly executable code for greater execution speed.
A comprehensive subroutine library is available.

programming aids

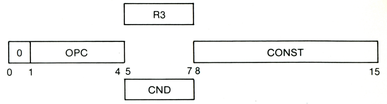
1k Stand-alone Update Package
This can update source text or object libraries; delete or insert source lines; and insert or omit object modules.

4k Debug Program
Interpretive debugging facilities are available to allow the user to trace the execution of his program and perform extensive diagnostic procedures.

4k Linkage Editor
This is a stand-alone processor that can output the end program on punched tape or magnetic tape. If all external references are satisfied it can also load the program into store during the linkage process.
The programmer can specify whether he requires link edit (program output) or link load (executable program in core), and which peripheral is to be used for the process. A number of control commands can be typed in at various stages of the process: for example, to specify an absolute loading address, to select certain programs from an object library, to terminate the output of the program; or to leave certain external references unsatisfied during a link edit.

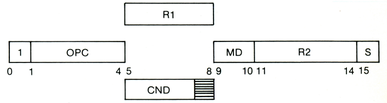
4k Text Editor
This allows the alteration, deletion and insertion of a character, group of characters, a line or a group of lines. The work is performed by manipulation of a text pointer over 'pages' of text which are held in core during an editing session. There are 17 elementary instructions ranging from 'reading a page into core' to a 'string search when the required string is not found on the specified page'. There are also 6 special action characters for certain operations, plus an auxiliary file feature for moving large portions of text.

Instruction formats
Format 0: Constant handling instructions



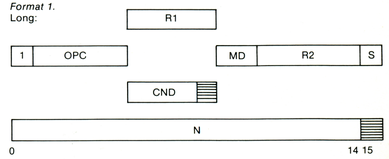
OPC – Operation code
R3 – Register on which operation has to be performed; *can be any of the first 8 general purpose registers.*
CND – Indicates condition for relative branches (coded in OPC)
CONST – 8-bit positive constant or displacement for branches. In some instructions this can be used as an OPC extension.

Format 1: Memory reference or register to register instructions.
Short:



OPC – Operation code
R1 – Specifies which of the 16 general purpose registers the operation is to be performed on.
CND – Same as format 0 instruction but bit 8 is not used.
R2 – Register number (1-14) relative to the second operand or to its *address.*
MD – Addressing mode.
S – This is used for memory reference instructions. If S = 0, the result goes to R1. *If S* = 1, the result goes to memory.

Format 1.
Long:



This is the same as the format 1 (short) instruction, except:
R2 – Register number (0-14) relative to the second operand or to its *address (for instance, as an index register).*
N – Constant, store address or displacement.